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PLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION N
10/043,898	01/11/2002	Takashi Ueda	10921.110US01	7265
7590 06/02/2004 Douglas P. Mueller MERCHANT & GOULD P.C.		EXAMINER		
			NGUYEN, DILINH P	
3200 IDS Center 80 South 8th Str	•		ART UNIT	PAPER NUMBER
Minneapolis, M			2814	
		•	DATE MAILED: 06/02/2004	· .

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
Office Action Summany	10/043,898	UEDA ET AL.	i
Office Action Summary	Examiner	Art Unit	
=	DiLinh Nguyen	2814	
The MAILING DATE of this communication appe Period for Reply	·		
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply if NO period for reply is specified above, the maximum statutory period with the set or extended period for reply will, by statute, any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be within the statutory minimum of thirty (30) of ill apply and will expire SIX (6) MONTHS fro cause the application to become ABANDO	e timely filed days will be considered timely. rom the mailing date of this communication.	í.
Status	•	·	
1) Responsive to communication(s) filed on 17 Fe	ebruarv 2004.		
_	action is non-final.		
3) Since this application is in condition for allowant	•	prosecution as to the merits is	
closed in accordance with the practice under Ex			
Disposition of Claims			
4)⊠ Claim(s) <u>1-6</u> is/are pending in the application.			
4a) Of the above claim(s) is/are withdraw	n from consideration		
5) Claim(s) is/are allowed.	II		
6)⊠ Claim(s) <u>1 and 3-6</u> is/are rejected.	,		
7)⊠ Claim(s) <u>2</u> is/are objected to.			
8) Claim(s) are subject to restriction and/or	election requirement.		
Application Papers	· ·		
9) The specification is objected to by the Examiner.			
10) The drawing(s) filed on is/are: a) acce		e Evaminer	
Applicant may not request that any objection to the di			
Replacement drawing sheet(s) including the correction) .
11)☐ The oath or declaration is objected to by the Exa			,-
Priority under 35 U.S.C. § 119			
 12) Acknowledgment is made of a claim for foreign p a) All b) Some * c) None of: 1. Certified copies of the priority documents 		a)-(d) or (f).	•
2. Certified copies of the priority documents		ation No	
3. Copies of the certified copies of the priorit			
application from the International Bureau		ved in this Hational Stage	-
* See the attached detailed Office action for a list of		ved.	
	·		
	,		
Attachment(s)			٠
Notice of References Cited (PTO-892)	4) Interview Summar	ry (PTO-413)	
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	Paper No(s)/Mail [5) Notice of Informal	Date Patent Application (PTO-152)	
Paper No(s)/Mail Date	6) Other:	, and	

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
- 2. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al. (U.S. Pat. 6229688) (newly cited).

Kobayashi et al. disclose a semiconductor device (fig. 5, column 5, lines 52 et seq.) comprising:

- a first lead 3 having an inner portion;
- a semiconductor chip 1 mounted on the inner portion of the first lead;
- a second lead 2 having an inner portion electrically connected to the semiconductor chip; and

a resin package 10 for sealing the semiconductor chip together with the inner portions of the first and second leads;

wherein at least the semiconductor chip has outer surfaces coated with a coating film 10 formed of amorphous fluororesin (polytetrafluoroethylene) (fig. 5, column 4, lines 62-63).

 Regarding claim 3, Kobayashi et al. disclose that the coating film 10 formed of polytetrafluoroethylene (column 4, lines 62-63). Art Unit: 2814

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (U.S. Pat. 6229688) (newly cited) in view of Sakai et al. (U.S. Pat. 5128209) (newly cited).

Kobayashi et al. substantially disclose all the limitations as claimed above except for the coating film has a thickness of 5-50 μm .

However, Sakai et al. disclose that a polytetrafluoroethylene film has a thickness of about 40 micrometers (column 3, lines 55-56). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Kobayashi et al. by having the coating film has the thickness of 40 micrometers with the structure as set forth above because as taught by Sakai et al., such the coating of polytetrafluoroethylene film has a thickness of about 40 micrometers would provide a good mechanical and chemical properties for the device (column 1, lines 45-46). Moreover, the thickness range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ

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233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed, Cir. 1990).

3. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (U.S. Pat. 6229688) in view of AAPA.

Kobayashi et al. substantially disclose all the limitations as claimed above except for the chip is an LED chip and resin package is formed of a transparent resin.

However, AAPA discloses that a semiconductor chip 1 is an LED chip (fig. 7, page 1, line 19) and a resin package 5 is formed of a transparent resin (fig. 7, page 1, lines 18-19). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Kobayashi et al. by having the LED chip and transparent resin with the structure as set forth above because as taught by AAPA (fig. 7), such the LED chip use in a display of a mobile phone as a light source or in a photointerrupter (page 1, lines 11-14) and the transparent epoxy resin is relatively inexpensive and is easily hardened by heating (page 2, lines 8-9).

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Allowable Subject Matter

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose the combination of a semiconductor device structure recited in the base claim, including the combination of the structure comprising: the semiconductor chip is electrically connected to the inner portion of the second lead via a wire, the coating film on the outer surfaces of the semiconductor chip also covering the wire and the inner portions of the first and second leads.

Therefore, the overall structure of the semiconductor device is neither anticipated nor rendered obvious over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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